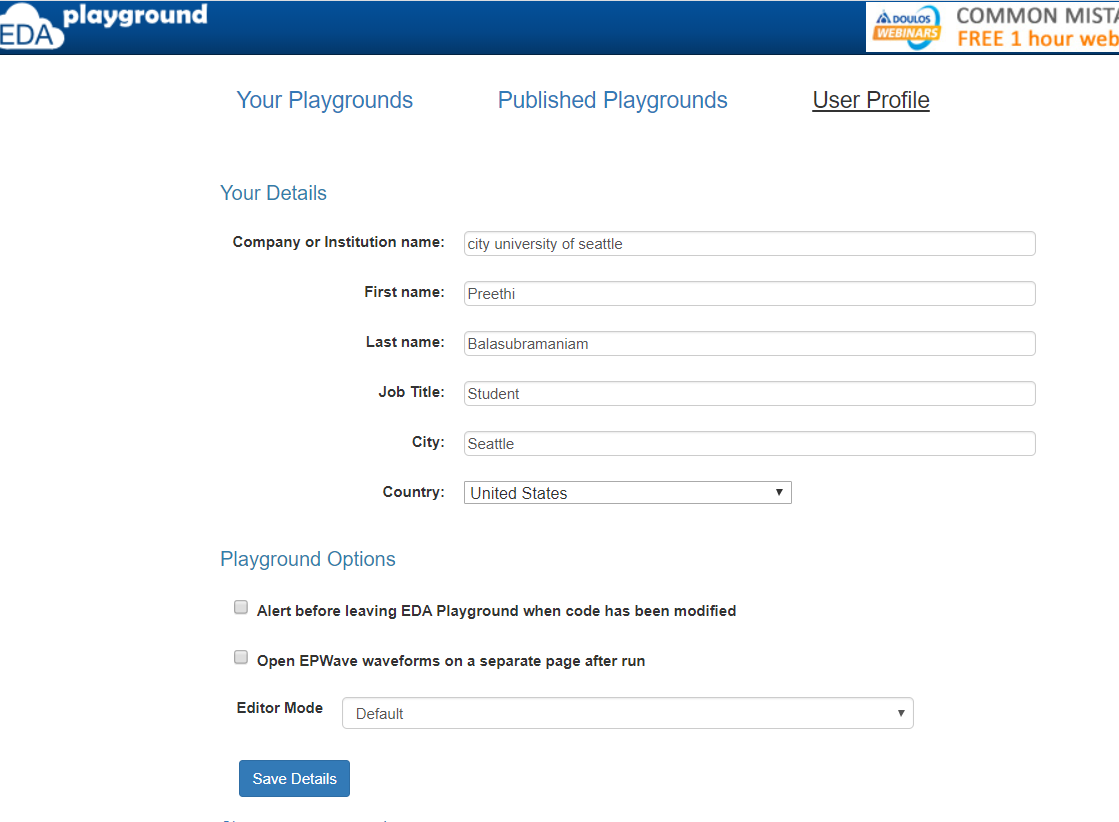
**Exercise Tasks:**

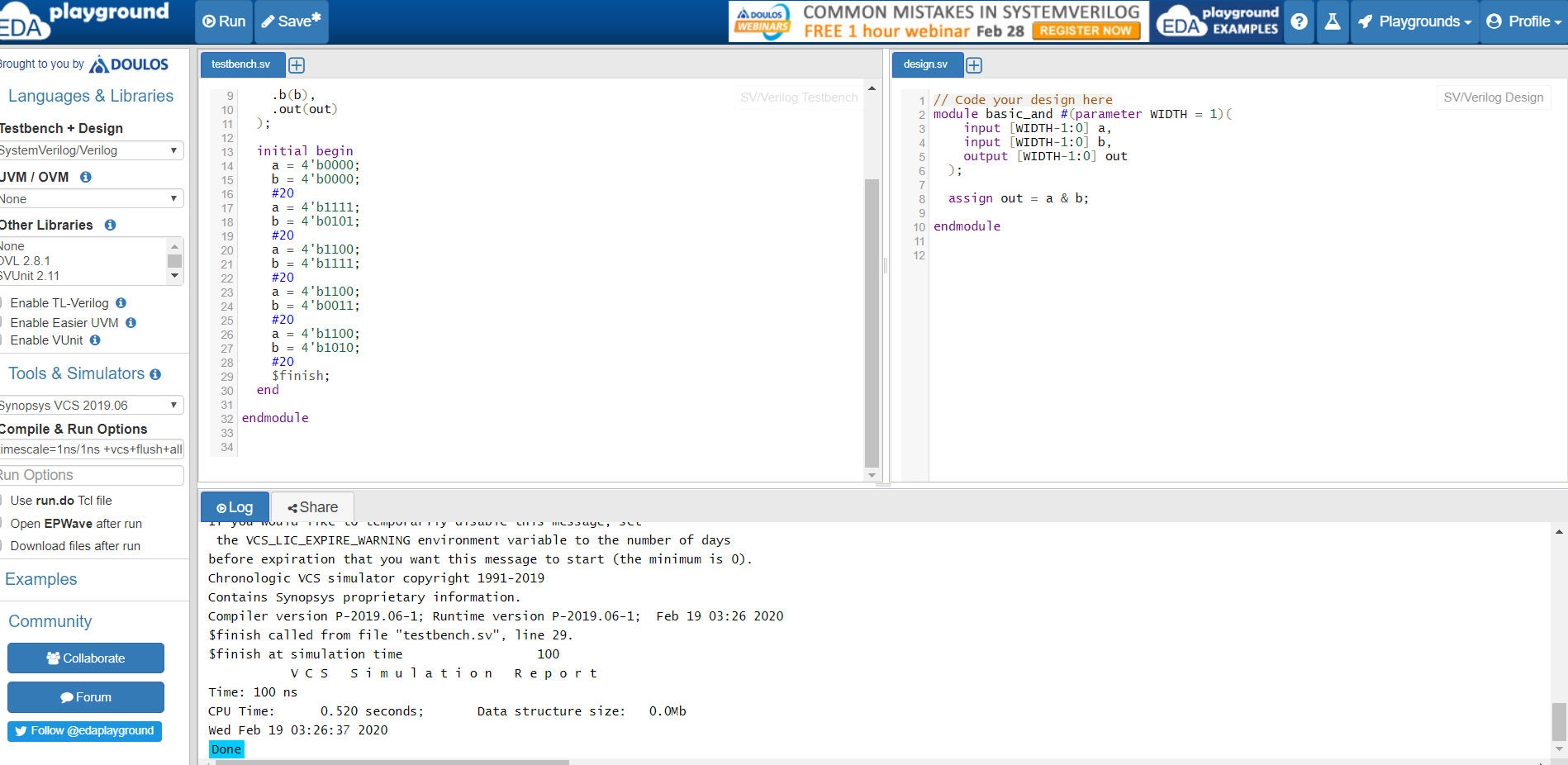
Using the online simulator: <https://www.edaplayground.com/>, Please

1. Register an account per Website above, by using your school email.

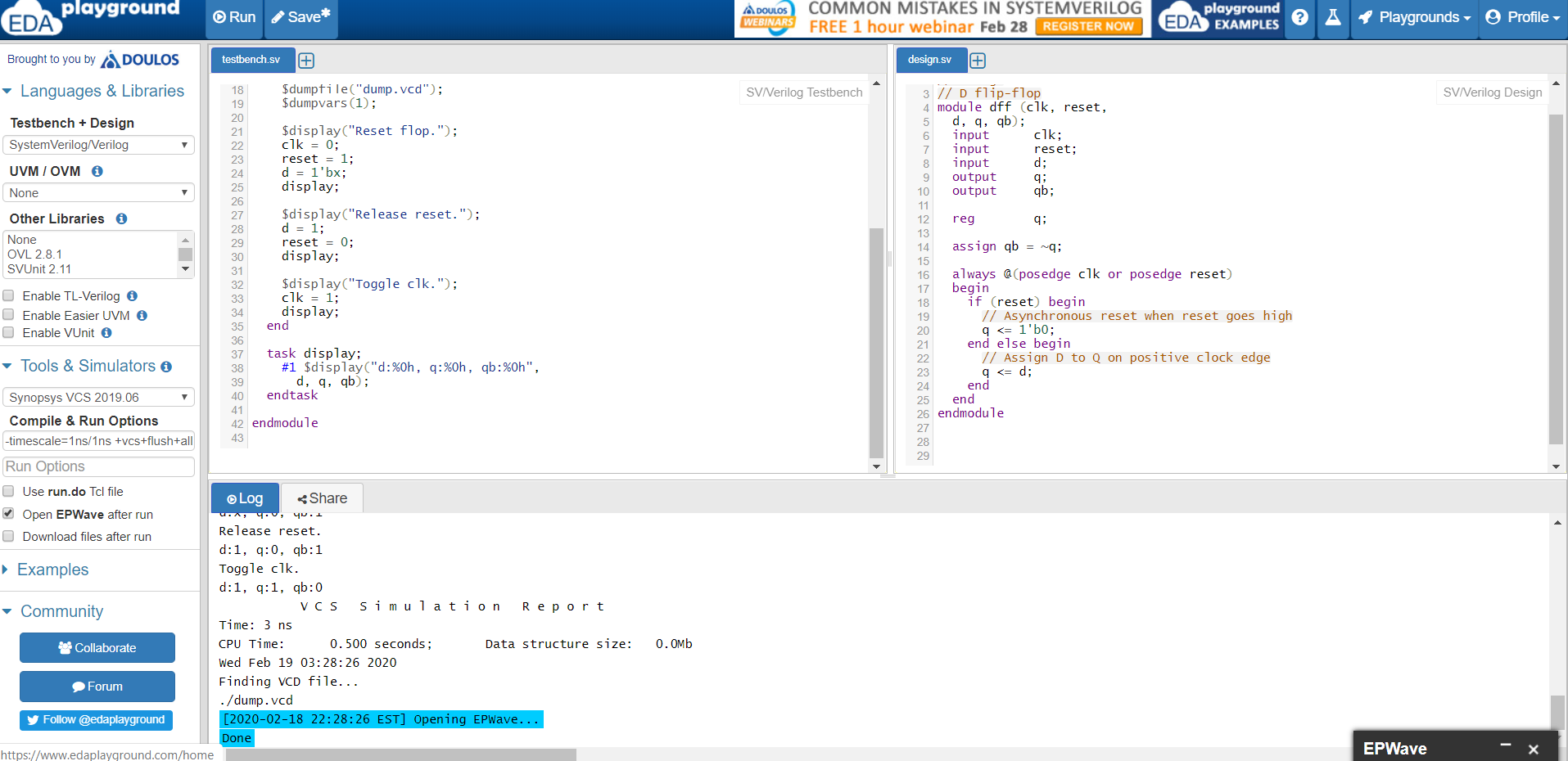
If the step above fails, STOP! You are to do the alternative Lab exercise (Found on this week’s Lab folder, title = “Inclass\_Excercise\_Search\_Verilog\_Simulator”

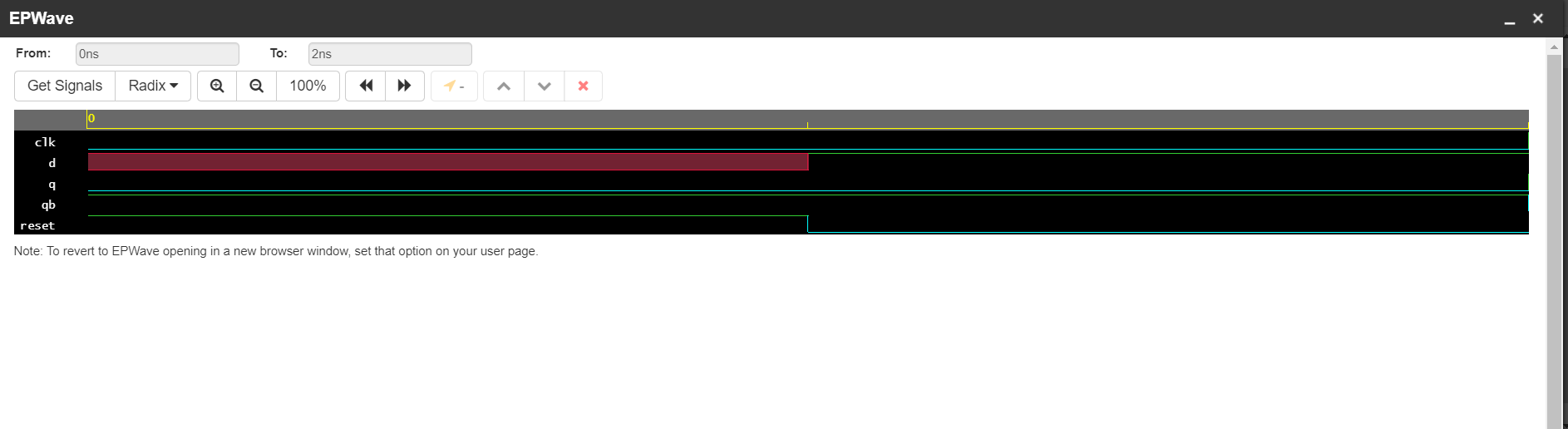


1. Simulate the “Verilog code for AND-Gate”, capture your simulation results (screen shot) below. E.g.

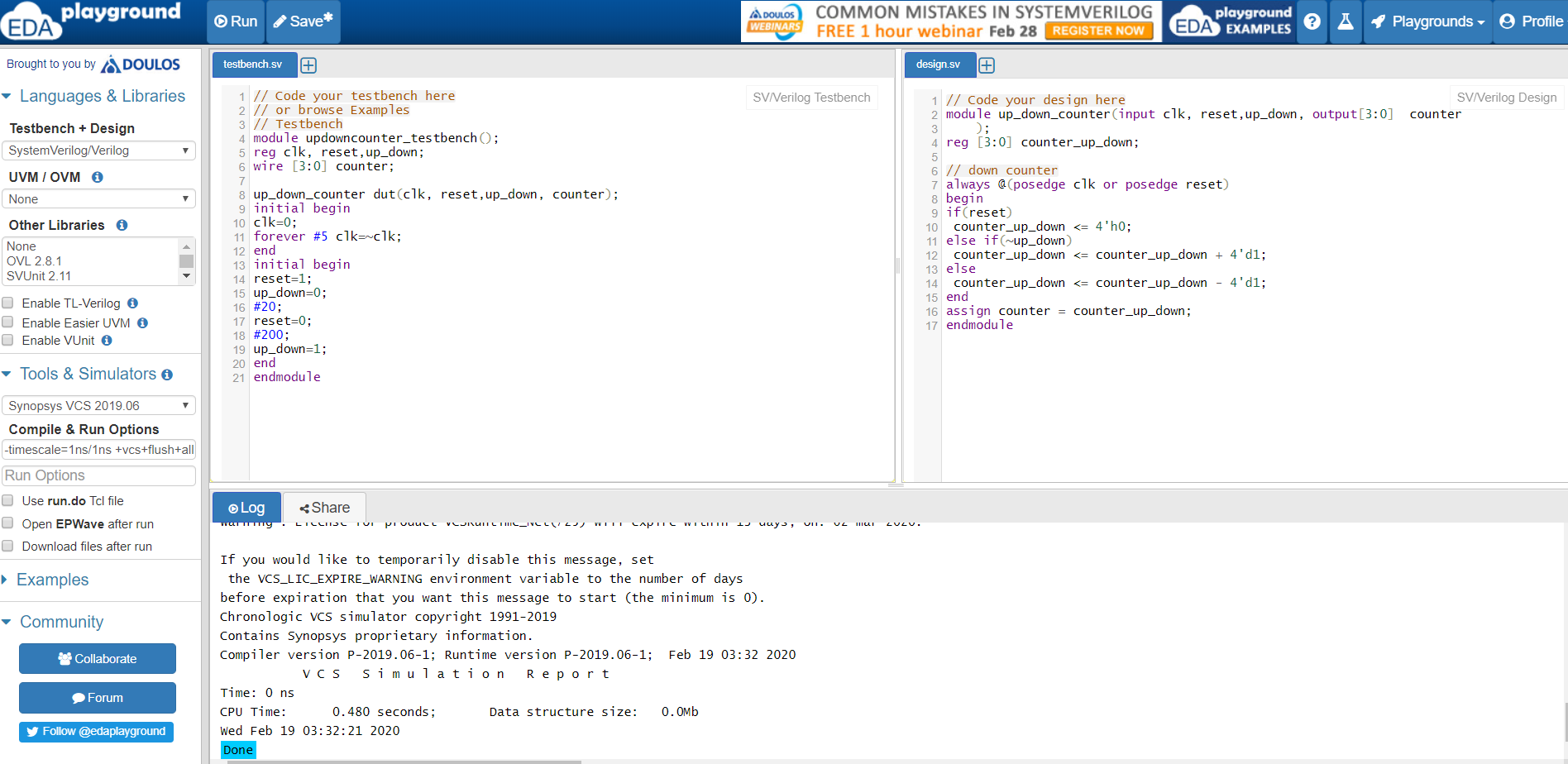


1. Simulate the “Verilog code for DFF, with VCS Simulator TB”, with the waveform display screen shot captured on the space below. The execution setup is shown below.

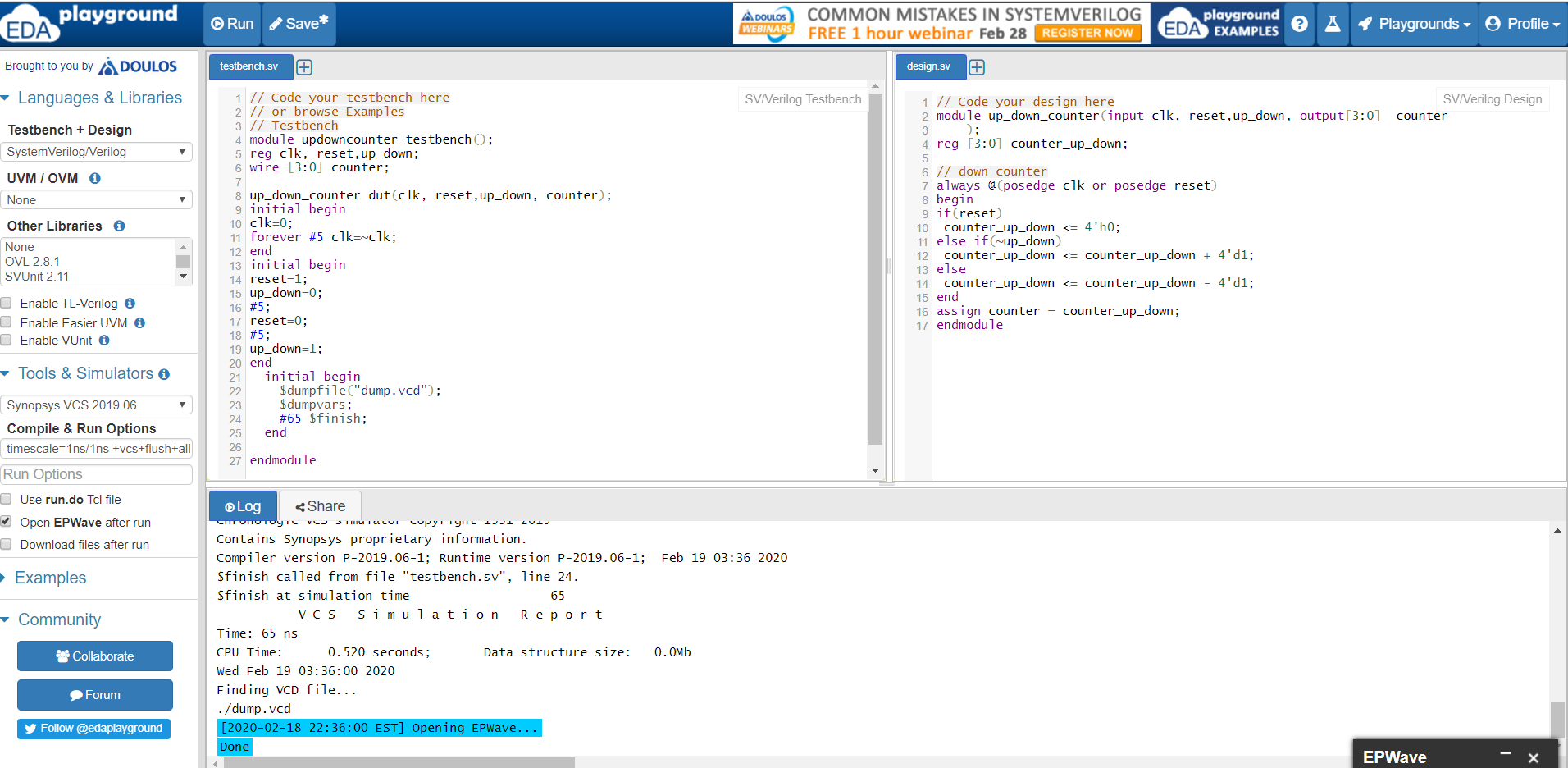




1. Referencing the “Verilog code for down counter”, make the following adjustments and execute.
2. Update the design codes, so the counter can count either up or down with the signal “up\_down” as input.



1. Adjust the corresponding testbench, so the VCS simulation can display the waveform of the simulation results.



1. Capture your simulation results (wave format) below. An example is shown below.

